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Wideband and Low Power CMOS Analog Multiplier in Deep Submicron Technology

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Abstract

In this paper CMOS Four Quadrant Analog Multiplier is designed. It is based on pair of common source amplifier, which acts as input transistor and two identical voltage controlled square root blocks which operate as nonlinear cancellation path. Simulated results using eldo spice in Mentor Graphics Tools for 350nm and 180nm CMOS technology. The main performances of the multiplier including bandwidth, power dissipation, and gain are improved.

Keywords: Analog Multiplier, Common Source Amplifier, Mentor Graphics, Square Root Bloc

Introduction

In analog signal processing the need often arises for a circuit that takes two analog inputs and produces an output proportional to their product. Such circuits are termed analog multiplier. So, the ideal output of the multiplier is $V_{out} = K_m.V_xV_y$, Where K_m = multiplier gain unit.

Four quadrant analog multipliers are very useful building blocks in many circuits such as adaptive filters, frequency shifters, and modulators. These applications are required to operate in low voltage environment for improving their power efficiency and incorporating with mixed signal systems to be used in portable application.

There are several means to realize a four quadrant analog multiplier and it is also suggested by that using saturated MOSFET in strong inversion is more practical than any other mean. Recently based on square law relation of Saturated MOSFET, various compact multiplier architectures. Most of them feature wide input range, high operating frequency and low power consumption which are resulted from excellent manipulation of the square law function in high compactness structure.

Focusing in this designed circuit, which is seemed to be compact circuit, it is found that the overall multiplier circuit cannot be called compact since it is require an extra voltage reference connected between the resistive loads .to generate the extra voltage reference, more power consumption and circuit complexity are unavoidable.

In this paper, we design a new multiplier which circuit have such a arrangement that transistor level improved such that the extra voltage reference becomes redundant and can be eliminated. We then obtain four quadrant analog multiplier

With real compact structure. Therefore the some circuit performance of the designed circuit is improved. In ordered to validate circuit performance, the designed multiplier has been simulated in eldo spice tool of Mentor Graphics using model parameter for 350nm and 180nm CMOS process. The
results shows that bandwidth, power dissipation and DC characteristics of the designed circuit.

The remaining of this paper is organized in the following section, a basic concept for realizing the analog multiplier is introduced in section II. Next a modification of square rooting circuit used to form an analog multiplier is described in section III. The multiplier is illustrated in section IV. In addition, simulated results of the multiplier and conclusion are presented in section V and VI respectively.

Basic Concept

Realizing analog multiplier is based on similar approach showing in Fig. 1. It comprises a pair of common source amplifier (M1 and M2), which acts as input transistor to provide output currents in term of squaring functions of input voltages (V1 and V2), and two identical square root blocks which operate as non- linear cancellation path. Injecting the output currents of the input transistors into the square root blocks, a differential output current of the overall circuit will become a multiplication function of two input signal V_{12} and V_{34}. More detail of mathematical analysis using

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square-law relation of saturated MOSFET in strong inversion will be shown in the paragraph below.

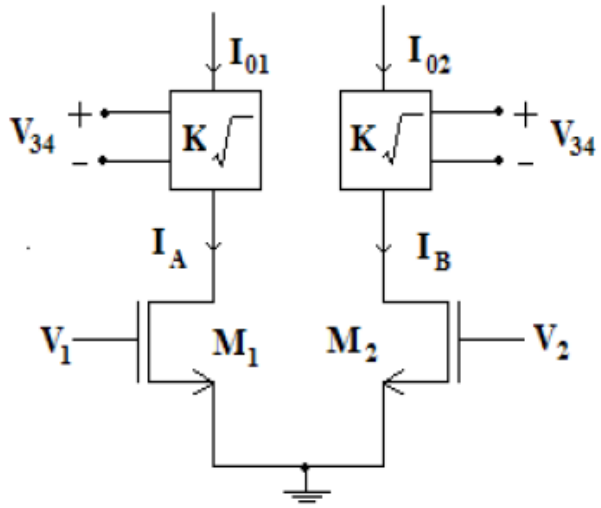

Figure 1. Basic concept of four quadrant analog multiplier[8]

Assuming MOSFET M1 and M2 are biased in active region and neglecting channel length modulation effect, the current I_A and I_B can be respectively found as,

$$I_A = K_n (V_1 - V_t)^2 \quad (1)$$

$$I_B = K_n (V_2 - V_t)^2 \quad (2)$$

Where $K = 0.5\,\mu_n C_{ox}\frac{W}{L}$ is a Trans conduction parameter of each MOSFET and Vt is the threshold voltage of NMOS transistor. From (1) and (2), the relation between the current I_A and I_B and the differential input voltage $V_{12} = V_1 - V_2$ can be given by

$$\sqrt{I_A} - \sqrt{I_A} = V_{12}\sqrt{K_n} \quad (3)$$

The drain current I_A and I_B are fed into the square rot blocks controlled by V_{34} , results in

$$I_{out} = I_{01} - I_{02} = K\ V_{34}\ (\sqrt{I_A} - \sqrt{I_A}) \quad (4)$$

Where K is the gain of square root blocks. Substituting (3) into (4), yields

$$I_{out} = K\sqrt{K_n} V_{34} V_{12} \quad (5)$$

It can be seen that an output current appeared in (5) is in form of a multiplication function between two input signal V_{12} and V_{34}. Based on this approach, both linear trans conductor and four quadrant analog multiplier have been designed.

Unfortunately, the early works in require more than 3v for supply voltage which is not sufficiently for modern analog design. Subsequently, a new square rooting circuit operated under 1.5V single supply was proposed in which can be applied as a compact four quadrant analog multiplier.

In next section, the improved square root circuit which is more suitable for realizing an analog multiplier will be described.

Square Rooting Circuit

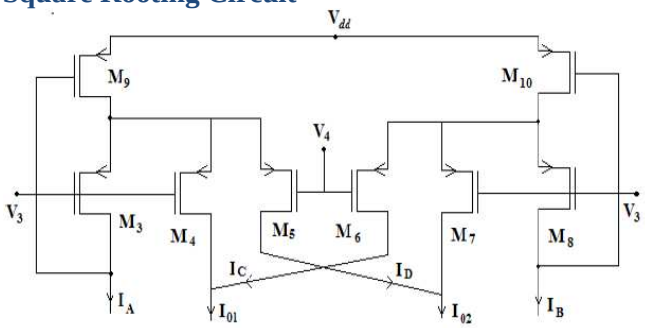

Figure 2. The square rooting circuit[8]

A square rooting circuit which is shown in Figure 2. Using square law relation of saturated MOSFET in strong inversion and setting M3-M8 to be identical, the current I_C and I_D are found to be

$$I_C = K_p\left(V_{34} + \sqrt{\frac{I_A}{K_B}}\right)^2 \quad (6)$$

$$I_D = K_p\left(V_{34} + \sqrt{\frac{I_B}{K_B}}\right)^2 \quad (7)$$

Where K_P is a Trans conduction parameter of each PMOS transistor and $V_{34} = V_3 - V_4$ is differential controlled voltage. Considering (4) and (5) in conjuction with the fact that $I_A + I_D = I_{01}$ and $I_B + I_C = I_{02}$ leading to

$$I_{01} = K_p {V_{34}}^2 + 2V_{34}\sqrt{K_p}\sqrt{I_A} + I_A + I_B \quad (8)$$

$$I_{02} = K_p {V_{34}}^2 + 2V_{34}\sqrt{K_p}\sqrt{I_B} + I_A + I_B \quad (9)$$

Subtracting (8) and (9), result in

$$I_{out} = I_{01} - I_{02} = 2\sqrt{K_p} V_{34}(\sqrt{I_A} - \sqrt{I_A}) \quad (10)$$

It is obvious that the output current of the improved square root circuit is function of I_A and I_B and its gain can be adjusted the voltage V_{34} and trans conduction parameter K_P.

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Schematic Circuit of Four Quadrant Analog Multiplier

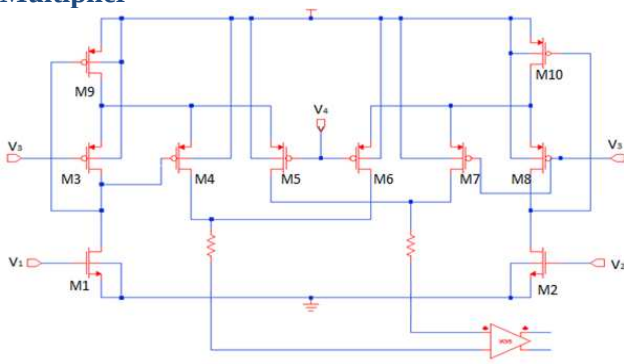

Figure 3. The four quadrant analog multiplier circuit[8]

Figure 3 shows that the multiplier circuit which is constituted by substituting the square rooting circuit in Fig. 2 into the square root blocks of Figure 1. Focusing on the differential output voltage we have found that

$$V_{out} = V_{01} - V_{02} = R\ (I_{01} - I_{02}) \qquad (11)$$

Also this V_{01} and V_{02} are fed in to the voltage controlled voltage source for generating the differential output of the V_{01} and V_{02}.

Substituting (10) into (11), differential output voltage can be found as

$$V_{out} = 2\ R\ V_{34}\sqrt{K_p}\ (\sqrt{I_A} - \sqrt{I_A}) \qquad (12)$$

Finally substituting (3) into (12) yields

$$V_{out} = 2\ R\ \sqrt{K_p K_n} V_{34} V_{12} \qquad (13)$$

Now, we have an output of four quadrant analog multiplier and its gain can be adjusted by the load resistor R and the dimension of each MOSFET.

Simulation Result

The simulation results are obtained in different topology 350nm and 180nm.

Simulation results in 350nm

The designed multiplier is simulated by using eldo spice for 350nm CMOS process parameter. The input V_{12} and V_{34} are set to be balance with common mode voltages of 0.5V, respectively and supply voltage VDD is set to 2.5V

A DC sweep showing the operation of the multiplier shown in Figure 4. The x-input, V_x is swept from -1 to +1, while at the same time the y-input is stepped from -1V to 1V in 0.5V increment.

Amplitude modulated signal is shown for information signal of 25M_{HZ} frequency and carrier of 60 M_{HZ} in Figure 5. An AC characteristics of the multiplier is shown in Figure 6 and Bandwidth comes out to be 229.70 M_{HZ}

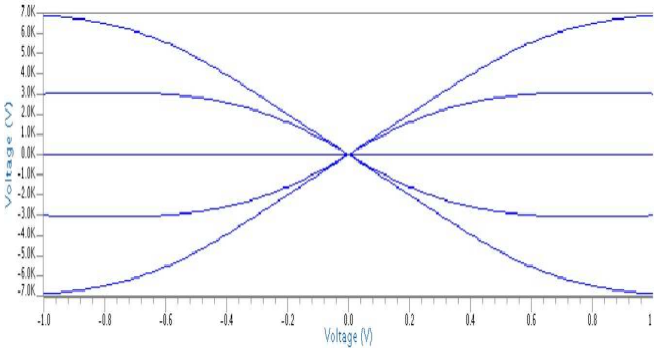

Figure 4. DC transfer characteristics in 350nm

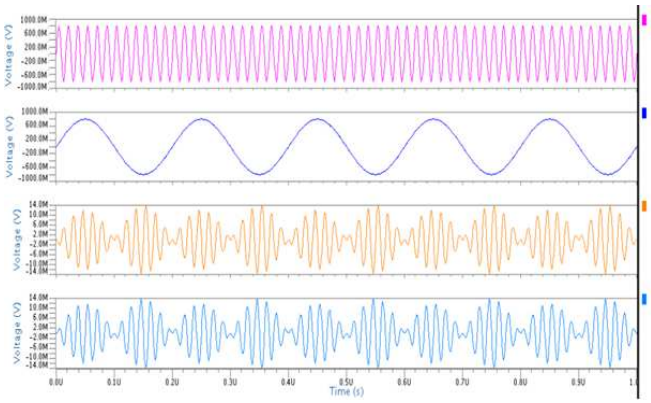

Figure 5. Transient response in 350nm

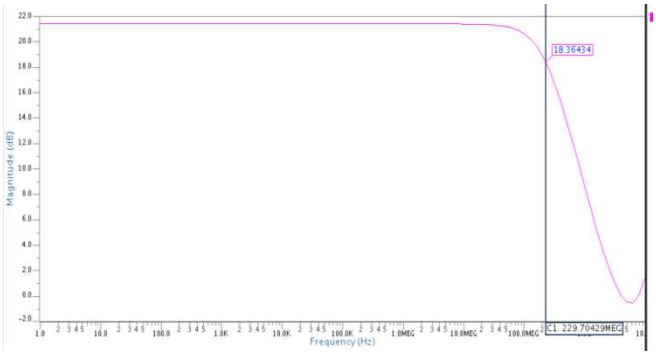

Figure 6.Frequency response in 350nm

Table 1. Different measured parameter in 350nm

Parameter	Value
Power supply(V)	2.5v
Bandwidth(M_{HZ})	229.70
Gain(dB)	18.36
Power dissipation(μW)	423.25

Simulation results in 180nm

The designed multiplier circuit is also simulated by

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using eldo spice for 180nm CMOS process parameter. The input voltage V_{12} and V_{34} are set to be balanced with common mode input voltage of 1V, respectively and supply voltage VDD is set to 1.8V.

A DC sweep showing the operation of the multiplier is shown in Figure 7. The x-input, V_x is swept from -1 to 1, while at the same time the y-input is stepped from -1V to 1V in 0.5V increment. Amplitude modulated signal is shown for information signal of 25M_{HZ} frequency and carrier of 60 M_{HZ} in Figure 8. An AC characteristic of the multiplier is shown in Figure 9and Bandwidth comes out to be 493.14 M_{HZ}.

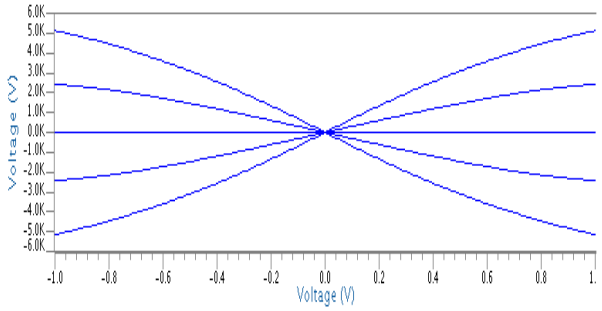

Figure 7. DC transfer characteristics in 180nm

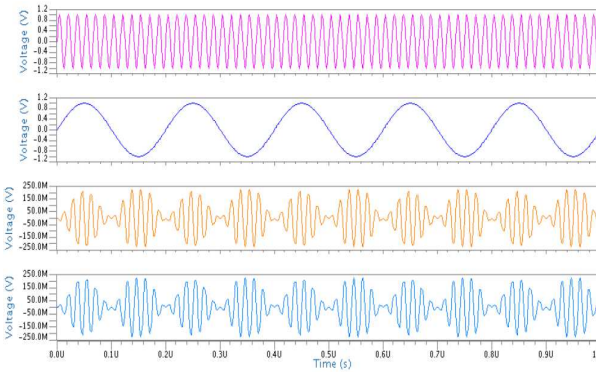

Figure 8. Transient response in 180nm

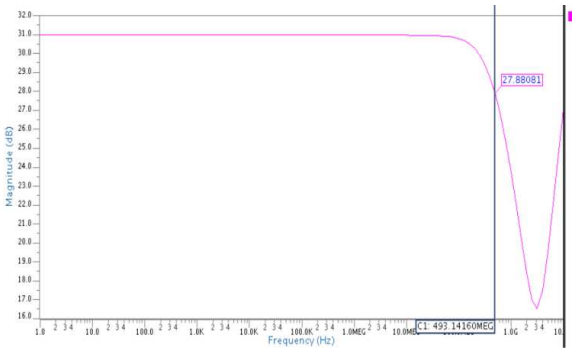

Figure 9. Frequency response in 180nm

Table 2.Different measured parameter in 180nm

Parameter	Value
Power supply(V)	1.5v
Bandwidth(M_{HZ})	493.14
Gain(dB)	27.88
Power dissipation(µW)	160.49

Conclusion

A new square rooting circuit can be used for realizing a CMOS four quadrant analog multiplier has been presented. The circuit is simulated in the Eldo Spice in Mentor Graphics Tool. The gain, bandwidth and power dissipation in 350nm CMOS technology are respectively 18.36 dB, 229.70 M_{HZ} and 423.25 µW. Also the circuit is simulated in 180nm CMOS technology and the gain, bandwidth and power dissipation are respectively 27.88dB, 493.14 M_{HZ} and 160.49 µW.

References

[1] *SmailHassouni, Hassan Qjidaa, Mohamed Latrach, "A DESIGN OF ANALOG VOLTAGE-MODE MULTIPLIER FOR UHF RFID PASSIVE IN 0.18UM CMOS PROCESS", Journal of Theoretical and Applied Information Technology, 20th July 2013. Vol. 53 No.2*

[2] *MeenakshiSuthar, Neha Gupta, Sapna Singh, PriyankaSoni, "Proposed Multiplier with Low Power and Efficient Performance",IACSIT Coimbatore Conferences vol. 28, Singapore 2012*

[3] *Sanjay Tembhurne, L. P. Thakare, "VLSI DESIGN OF FOUR QUADRANT ANALOG MULTIPLIER FOR ISM BAND", The International Journal of Computer Science & Applications, Volume 1, No. 3, May 2012*

[4] *Nandini A.S, SowmyaMadhavan and DrChirag Sharma, "DESIGN AND IMPLEMENTATION OF ANALOG MULTIPLIER WITH IMPROVED LINEARITY", International Journal of VLSI design & Communication Systems, Vol.3, No.5, October 2012*

[5] *PriyankaMandavgade, RupaliBalpande, "VlSI Implementation Of An Analog Multiplier", IRNet Transactions on Electrical and Electronics Engineering (ITEEE) ISSN 2319 – 2577, Vol-1, Iss-2, 2012*

ISSN: 2277-9655
Impact Factor: 1.852

[6] *Soliman A. Mahmoud, "Low Voltage Low Power Wide Range Fully Differential CMOS Four-Quadrant Analog Multiplier", 978-1-4244-4480-9/09/$25.00 ©2009 IEEE*

[7] *Yuan Gao, KaizhiCai, YuanjinZheng and Ban-Leong Ooi, "A Wideband CMOS Multiplier for UWB Application" 1-4244-0521l-1/07/$20.00 ©2007 IEEE*

[8] *N. Kiatwarin, W. Ngamkham and W. Kiranon, "A Compact Low Voltage CMOS Four Quadrant Analog Multiplier", ECTI International Conference,2007*

[9] *BoonchaiBoonchu, WanlopSurakampontorn, "A New NMOS Four-Quadrant Analog Multiplier", 0-7803-8834-8/05/$20.00 ©2005 IEEE.*

[10] *Chandra shekhar,Mr. AjaiGautam, SaurabhChitransi, "Low Voltage Low Power Gilbert Cell based Multiplier Circuit", International Journal of Engineering Research and Applications, Vol. 1, Issue 1, pp.011-014*

[11] *R. Jacob Baker, Harry W. Li and David E. Boyce, "CMOS Circuit Design, Layout, and Simulation", TK 7871.99 .M44B335 1998 C.1*

[12] *Phillip E. Allen and Doaglas R. Holberg, "CMOS Analog Circuit Design", Second edition, New york Oxford University Press, 200*

[13] *BehzadRazavi, "Design of Analog CMOS Integrated Circuits", ISBN 0-07-238032-2, TK7874.654.R39 2001*